

REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 1-2, 5-7, 9-10, 13-17, 19-25, and 27-28 are now in this application. Claims 5, 9, 13, 17, 20, and 22 have been amended. (Claim 22 was amended to correct an informality.) Claims 3, 4, 8, 11-12, 18, and 26 have been cancelled.

The Examiner objected to the amendment mailed on March 15, 2002 under 35 U.S.C. §132 as introducing new matter into the disclosure. In objecting to the amendment, the Examiner indicated that there is support for the formation of a layer of third material over a planarized layer of material, but argued that there is no support for a layer of material 342 that lowers resistance.

The Examiner objected to the amendment mailed on March 4, 2003 under 35 U.S.C. §132 as introducing new matter into the disclosure. In objecting to the amendment, the Examiner argued that there is no support in the specification for the limitations in claim 22 that require that the third layer of material lower the resistance of the first material. In addition, the Examiner argued that there is no support in the specification for the limitations in claim 25 that require that the layer of third material be selectively etched during the selective etching process. Further, the Examiner argued that there is no support in the specification for the limitation in claim 26 that the third layer of material is conductive.

The Examiner rejected claims 19-23 and 25-26 under 35 U.S.C. §112, first paragraph. In rejecting the claims, the Examiner argued that no support in the specification for the limitations in claim 22 that require that the third layer of material lower the resistance of the layer of first material. In addition, the Examiner argued that there is no support in the specification for the limitations in claim 25 that require that the layer of third material be selectively etched during the selective etching process. Further, the Examiner argued that there is no support in the specification for the limitation in claim 26 that the third layer of material is conductive.

With respect to each of the above rejections which are based on the argument that the specification does not teach a third layer of material that lowers the resistance of the layer of first material, applicant respectfully directs the Examiner to applicant's specification, page 5, lines 13-16, which recites,

“After this, as shown in FIG. 3B, oxide layer 330 and polysilicon layer 320 are chemically-mechanically polished until oxide layer 330 is substantially, completely removed from the surface of polysilicon layer 320 to form a planarized layer of polysilicon.”

Thus, applicant’s specification teaches that polysilicon layer 320, which can be read to be a layer of first material, and oxide layer 330, which can be read to be a layer of second material, are chemically-mechanically polished to form a planarized layer of polysilicon.

In addition, applicant’s specification also recites,

“Alternately, after the planarization step, one or more additional layers of material, such as materials which lower the resistance of polysilicon, can be formed over layer 340.” (See page 5, lines 25-27.)

Thus, if one additional layer of material is used, the one additional layer of material can be read to be a third layer of material, and can be described as a layer of material 342. In addition, since the one additional layer of material lowers the resistance of polysilicon, and polysilicon layer 320 can be read to be the layer of first material, then the one additional layer of material can be read to be a third layer of material that lowers the resistance of the layer of first material.

Thus, applicant’s specification teaches a layer of third material that lowers the resistance of the layer of first material. As a result, the amendment mailed on March 15, 2002 and the amendment mailed on March 4, 2003 do not introduce new matter into the disclosure with respect to the third layer of material lowering the resistance of the layer of first material. For the same reasons, claims 19-23 and 25 satisfy the requirements of the first paragraph of 35 U.S.C. §112 with respect to the third layer of material lowering the resistance of the layer of first material. (Claim 26 has been cancelled.)

With respect to each of the above rejections which are based on the argument that the specification does not teach that the layer of third material is selectively etched during the selective etching process, applicant respectfully directs the Examiner to applicant’s specification, from page 5, line 27 to page 6, line 1, which recites,

“The mask is then formed and patterned on the additional layers of material which are then etched along with planarized polysilicon layer 340 to form the structures (e.g., local interconnect lines).”

As noted above, one additional layer of material can be read to be the third layer of material. As just noted, an additional layer of material (the layer of third material) can be etched with planarized polysilicon layer 340, which can be read to be the layer of first material. Thus, applicant’s specification teaches that the layer of third material and the layer of first material can be etched at the same time. As a result, the amendment mailed on March 4, 2003 does not introduce new matter into the disclosure with respect to the layer of third material and the layer of first material being selectively etched. For the same reasons, claims 19-23 and 25-26 satisfy the requirements of the first paragraph of 35 U.S.C. §112 with respect to the layer of third material and the layer of first material being selectively etched.

With respect to each of the above rejections which are based on the argument that the specification does not teach that the third layer of material is conductive, applicant notes that claim 26 has been cancelled. Applicant’s specification indirectly teaches that the third layer of material is conductive. However, in the interests of furthering prosecution, claim 26 has been cancelled.

The Examiner also rejected claims 5, 13, and 20 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant disagrees that the phrase “a value” lacks clarity. However, in the interests of furthering prosecution, claims 5, 13, and 20 have been amended and are believed to satisfy the requirements of the second paragraph of section 112.

The Examiner rejected claims 1, 2, 5-7, 10, 13-16, and 19-28 under 35 U.S.C. §102(e) as being anticipated by Li et al. (U.S. Patent No. 6,162,368). For the reasons set forth below, applicant respectfully traverses this rejection.

Claim 1 recites, in part,

“forming a layer of first material . . . ;
“forming a layer of second material on the top surface of the layer of first material; and
“chemically-mechanically polishing the layer of second material and the underlying layer of first material with a slurry until the layer of second material is

substantially all removed from the layer of first material to form the planarized layer of material, the planarized layer of material lying over the wafer upper levels and the wafer lower level.”

In rejecting the claims, the Examiner pointed to the step of forming the layer of polysilicon 16 as constituting the step of forming a layer of first material, and the step of forming native oxide layer 18 as constituting the step of forming a layer of second material. The Examiner also argued that the Li reference teaches the chemical-mechanical polishing step required by the claims.

Applicant notes that the Li reference teaches two chemical-mechanical polishing steps: a first step that uses slurry 50a to remove native oxide layer 18, and a second step that uses slurry 50b to remove polysilicon layer 16. However, neither of the two chemical-mechanical polishing steps taught by Li can be read to be the chemically-mechanically polishing step required by claim 1.

The first chemical-mechanical polishing step of Li, which uses slurry 50a, can not be read to be the chemical-mechanical polishing step of claim 1 because the first chemical-mechanical polishing step of Li (slurry 50a) does not “form the planarized layer of material” as required by claim 1. Claim 1 requires that the chemical-mechanical polishing step be performed “until” the layer of second material is substantially all removed from the layer of first material to form the planarized layer of material.

As shown in FIG. 2C of Li, after all of the native oxide layer 18 (the layer of second material) has been removed from polysilicon layer 16 (the layer of first material) with slurry 50a, the remaining layer of polysilicon 16 (the layer of first material) still has a severe non-planar topology. Thus, the first chemical-mechanical polishing step of Li (slurry 50a) does not form a planarized layer of material, but instead exposes the severe topology of polysilicon layer 16. As a result, the first chemical-mechanical polishing step of Li (slurry 50a) can not be read to be the chemical-mechanical polishing step of claim 1.

In addition, the second chemical-mechanical polishing step of Li, which uses slurry 50b, can not be read to be the chemical-mechanical polishing step of claim 1 because the second chemical-mechanical polishing step (slurry 50b) is not performed “until” the layer of second material (native oxide layer 18) is substantially all removed from the layer of first material (polysilicon layer 16) as required by claim 1.

As shown in FIG. 2C, the native oxide layer 18 is already gone before the second chemical-mechanical polishing step of Li begins, before polysilicon layer 16 is etched with slurry 50b. As a result, it is not possible for the second chemical-mechanical polishing step of Li to be performed “until” the layer of second material (native oxide layer 18) is substantially all removed from the layer of first material (polysilicon layer 16). Thus, the second chemical-mechanical polishing step of Li (slurry 50b) can not be read to be the chemical-mechanical polishing step of claim 1.

Therefore, since neither of the two chemical-mechanical polishing steps disclosed by Li teach or suggest the limitations required by the chemical-mechanical polishing step of claim 1, claim 1 is not anticipated by Li. In addition, since claims 2, 5-7, 10, and 13-16 depend either directly or indirectly from claim 1, claims 2, 5-7, 10, and 13-16 are not anticipated by Li for the same reasons as claim 1.

With respect to claim 22, this claim recites, in part,

“forming a layer of third material on the planarized layer of first material, the third layer of material lowering a resistance of the first layer of material.”

In rejecting claim 22, the Examiner pointed to the step of forming layer 102 as constituting the step of forming a layer of third material. However, the structure shown in FIGs. 2B and 2C that is identified by reference numeral 102 is not a layer of material, but is instead the rough surface 102 of outer polishing pad 106. (See column 3, lines 12-15 of Li.) Thus, since Li fails to teach or suggest the formation of a layer of third material, claim 22 is not anticipated by the Li reference. In addition, since claims 19-21 and 23 depend from claim 22, claims 19-21 and 23 are not anticipated by Li for the same reasons as claim 22.

With respect to claim 24, this claim recites, in part,

“selectively etching the planarized layer of material that covers the wafer upper levels and the wafer lower level of the top surface of the wafer.”

In rejecting claim 24, the Examiner stated, with reference to the selectively etching step, “selectively etching the planarized layer of material that covers (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).” Applicant respectfully has been unable to identify the steps in Li that the Examiner believes reads on the selectively etching step, and has been

otherwise been unable to find any discussion in Li that teaches or suggests that polysilicon layer 16 (the layer of first material) is selectively etched when polysilicon layer 16 covers the upper levels of regions 14 as required by claim 24. As a result, claim 24 is not anticipated by Li. In addition, since claims 25 and 27-28 depend either directly or indirectly from claim 24, claims 25 and 27-28 are not anticipated by Li for the same reasons as claim 24.

The Examiner objected to claims 9 and 17, but indicated that these claims would be allowable if amended to be in independent form and to include all of the limitations of the base claim and any intervening claims. Claims 9 and 17 have been amended to be in independent form and are believed to include all of the limitations of the base claims (claims 9 and 17 depending directly from claim 1).

Thus, for the foregoing reasons, it is submitted that all of the claims are in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are respectively requested.

Respectfully submitted,

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AMENDMENTS TO THE CLAIMS

1. (Previously Amended) A method for forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having spaced-apart wafer upper levels and a wafer lower level that lies between the wafer upper levels, the wafer upper levels lying above the wafer lower level, the method comprising the steps of:

forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level;

forming a layer of second material on the top surface of the layer of first material; and chemically-mechanically polishing the layer of second material and the underlying layer of first material with a slurry until the layer of second material is substantially all removed from the layer of first material to form the planarized layer of material, the planarized layer of material lying over the wafer upper levels and the wafer lower level.

2. (Original) The method of claim 1 wherein the first lower level lies above the wafer upper level.

3. Cancelled.

4. Cancelled.

5. (Currently Amended) The method of claim 2 wherein the planarized layer of material has a first thickness over the wafer upper level, and

wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a ~~value~~ second thickness that is equal to a greater than the first thickness.

6. (Original) The method of claim 1 wherein the first material is polysilicon.

7. (Original) The method of claim 1 wherein the second material is oxide.

8. Cancelled.

9. (Currently Amended) ~~The method of claim 1 wherein~~ A method for forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having spaced-apart wafer upper levels and a wafer lower level that lies between the wafer upper levels, the wafer upper levels lying above the wafer lower level, the method comprising the steps of:

forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level;

forming a layer of second material on the top surface of the layer of first material; and chemically-mechanically polishing the layer of second material and the underlying layer of first material with a slurry until the layer of second material is substantially all removed from the layer of first material to form the planarized layer of material, the planarized layer of material lying over the wafer upper levels and the wafer lower level, the slurry has having a selectivity that falls within an approximate range of 0.9-1.1:1.

10. (Original) The method of claim 2 and further comprising the step of forming a layer of third material on the planarized layer of material.

11. Cancelled.

12. Cancelled.

13. (Currently Amended) The method of claim 10 wherein the planarized layer of material has a first thickness over the wafer upper level, and wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a ~~value~~ second thickness that is equal to a greater than the first thickness.

14. (Original) The method of claim 1 and further comprising the step of doping the layer of first material prior to forming the layer of second material.

15. (Original) The method of claim 1 wherein the layer of first material is doped polysilicon.

16. (Previously Amended) The method of claim 1 wherein the layer of first material makes an electrical contact with a device on the wafer.

17. (Currently Amended) ~~The method of claim 1 wherein~~ A method for forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having spaced-apart wafer upper levels and a wafer lower level that lies between the wafer upper levels, the wafer upper levels lying above the wafer lower level, the method comprising the steps of:

forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level;

forming a layer of second material on the top surface of the layer of first material, the second layer of material is being thicker than the layer of first material; and

chemically-mechanically polishing the layer of second material and the underlying layer of first material with a slurry until the layer of second material is substantially all removed from the layer of first material to form the planarized layer of material, the planarized layer of material lying over the wafer upper levels and the wafer lower level.

18. Cancelled.

19. (Previously Amended) The method of claim 22 wherein the first lower level lies above the wafer upper level.

20. (Currently Amended) The method of claim 19 wherein the planarized layer of first material has a first thickness over the wafer upper layer, and

wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a ~~value~~ second thickness that is equal to or greater than the first thickness.

21. (Previously Amended) The method of claim 22 wherein the first material is doped polysilicon.

22. (Currently Amended) A method of planarizing a layer of semiconductor material on a processed wafer, the wafer having a top surface, the top surface having a wafer lower level and a wafer upper level that lies above the wafer lower level, the method comprising the steps of:

forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level;

forming a layer of second material on the top surface of the layer of first material; and chemically-mechanically polishing the layer of second material and the underlying layer of first material until the layer of first material is substantially planar to form a planarized layer of first material, the planarized layer of first material covering the wafer upper level of the top surface of the wafer; and

forming a layer of third material on the planarized layer of first material, the third layer of material lowering a resistance of the first layer of material.

23. (Previously Amended) The method of claim 22 wherein the layer of first material makes an electrical contact with a device on the wafer.

24. (Previously Added) A method of forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having spaced-apart wafer upper levels and a wafer lower level that lies between the wafer upper levels, the wafer upper levels lying above the wafer lower level, the method comprising the steps of:

forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level;

forming a layer of second material on the top surface of the layer of first material;
chemically-mechanically polishing the layer of second material and the underlying layer of first material until the layer of first material is substantially planar to form a planarized layer of material, the planarized layer of material covering the wafer upper levels and the wafer lower level of the top surface of the wafer; and

selectively etching the planarized layer of material that covers the wafer upper levels and the wafer lower level of the top surface of the wafer.

25. (Previously Added) The method of claim 24 and further comprising the step of forming a layer of third material on the planarized layer of material, the layer of third material and the layer of first material being selectively etched during the selectively etching step.

26. (Cancelled).

27. (Previously Added) The method of claim 24 wherein the layer of first material and the layer of second material are etched with a slurry that etches the layer of first material and the layer of second material at approximately a same rate.

28. (Previously Added) The method of claim 24 wherein all of the layer of second material is removed during the chemically-mechanically polishing step.